UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,374	03/26/2004	Munehiro Uratani	1248-0709PUS1	7619

2292 7590 08/09/2007
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
08/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/809,374	URATANI ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 8, 9* is/are rejected.

7)☐ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 8-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(1) Regarding claim 8:

Claim 8 recites a program that including a signal timing adjustment device, it is unclear whether claim 8 is directed to a program or a device.

(2) Regarding claim 9:

Claim 9 recites a computer-readable storage medium storing a timing adjustment amount setting program including a signal timing adjustment device, it is unclear whether claim 9 is directed to a computer-readable medium or a device.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 8 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 8 recites a signal timing adjustment amount setting program. It appears that the claim would reasonable be interpreted by one of ordinary skill in the art as software per se. Software per se, i.e., the description or expression of the program, is not physical "things". They are neither computer components nor statutory processes, as they are not "act" being performed. Therefore, it is a non-statutory functional descriptive material.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US 6,424,184 B1) in view of Yamada (US 5,912,591).

(1) Regarding claim 1:

Yamamoto et al. discloses a device comprising:

a voltage generating section for generating a plurality of adjustment voltage (the resistor 332 in figure 6, one end of the resistor 332 is connected to the power supply voltage Vc, and the other end of the resistor 332 is connected to the ground voltage. The voltage at point R1 through R5 of the resistor 332 are respectively supplied to the

switch circuit 333 as voltage V1 through V5in accordance with a resistance division method, column 11, line 66 – column 12, line 5).

a voltage selection section (control circuit 331 in figure 6) for selecting, from the plurality of adjustment voltages, an adjustment voltage that is in accordance with a delay-time adjustment amount (the multiplexers 331m-1 through 331m-5 each select data to be stored in the D flip-flop corresponding thereto in accordance with the level of the determination signal K1, column 11, lines 11-14, the control signals S1 through S5 are respectively used fro turning on or off the switch elements 333-1 through 333-5, only the switch elements corresponding to the control signals at a high level are turned on, and the voltages corresponding to such switch elements are selected, column 12, lines 9-14), which is set so that delay time of each circuit block in a integrated circuit becomes closer to an average value of the delay time, the delay time being time between an input of data to the circuit block and an output of the data from the circuit block (objective of the present invention is to provide a method for adjusting input and output characteristic of the frequency-voltage conversion circuit of the system, column 1, lines 42-44); and

Yamamoto et al. fails to disclose a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage change in accordance with a value of the adjustment voltage selected.

However, Yamada discloses a delay circuit that apply back biases to a transistor, by that the threshold voltage of the transistor are raised and the delay time is increase (column 10, lines 21-61).

It is desirable to have a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage change in accordance with a value of the adjustment voltage selected because it can the size of the device because any MOS field effect transistor with large gate wide are never required (column 26, lines 28-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Yamada in the device of Yamamoto et al. to reduce the size of the device.

(2) Regarding claim 2:

Yamamoto et al. further disclose a delay measurement section for measuring the delay time (delay amount determination circuit 32 in figure 32, column 10, lines 40-50).

(3) Regarding claim 4:

Yamada further discloses that a well of the transistor is separated from a well of another circuit that is formed on a same substrate; and the adjustment voltage (back bias voltage) selected is applied to the well of the transistor (the individual transistors are formed in the different well which are electrically isolated from one another so that the back bias control unit is capable of applying back bias voltage to the individual well separately whereby the threshold voltage of the individual transistors formed in the individual wells are independently and separately controllable, column 10, lines 54-61 and column 13, lines 25-32).

(4) Regarding claim 5:

Yamamoto et al. discloses that the signal timing adjustment device being contained in the integrated circuit (the system 1 in figure 1 can be formed on a single semiconductor chip, column 7, lines 49-55).

(5) Regarding claim 6:

Yamamoto et al. further discloses a fixing section for fixing the delay-time adjustment amount (the switch section 333 in figure 6 will be turn on or off by the control signal and fix the output signal, column 12, line6-14).

Allowable Subject Matter

7. Claims 7 is allowed.

8. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mullarkey (US 2001/0049797 A1) discloses a method and apparatus for adjusting data delay. Yamauchi (US 5,251,172) discloses a semiconductor memory apparatus having reduced amount of line amplification delay. Lutkemeyer (US 6,501,311 B2) discloses a system and method for compensating for supply voltage induced signal delay mismatched. Seki et al. (US 6,657,467 B2) discloses a delay control circuit with internal power supply voltage control. Yamauchi

(US 6,711,044 B2) discloses a semiconductor memory device with a countermeasure to a signal delay.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee

Examiner
Art Unit 2611
7/25/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER